IN THE SPECIFICATION:

Please amend the specification to read as follows:

Replace the paragraph starting at page 6, line 3 with this paragraph:

B'

FIG. 1 is a plan diagram illustrating an embodiment of a layout of a gate array architecture in accordance with the present invention. This particular gate array architecture includes a capacitance improved layout. Therefore, each row of "regular" or full" sized transistors, the larger transistors is this embodiment, is complemented ~~with row~~ with a row of "small" transistors, the smaller transistors in this embodiment, which may be used for clock buffering and to create logic gates that will consume less power compared with full or regular sized transistors. Therefore, in this particular embodiment, two separate and distinct sizes of transistors are employed so that the smaller of the two may be applied to operations that typically consume significant or greater amounts of power.